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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,943	12/15/2003	Wei Chen	TI-36101	3708

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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,943	CHEN ET AL.	
	Examiner	Art Unit	
	Adi Amrany	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 18-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 18 and 32 are rejected because the limitation of "a mapping" is indefinite. The specification discloses that the mapping may be any combination of coupling of the voltage source outputs (paragraph 46). The mapping may be simple or complex, may couple none, some or all of the outputs, and may be predetermined or determined dynamically. This limitation in the claims is indefinite.

Claims 19-31 and 33-36 are rejected because they depend on claims 18 and 32, respectively, and therefor, contain the rejected limitation of "a mapping."

For the purposes of the art rejections of claims 18-36, the mapping will be interpreted as a simple, predetermined coupling of all of the voltage sources.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Bardeen (US 2,524,035). Bardeen discloses a circuit comprising:

two voltage sources (figure 1, items 7 and 8; column 9, lines 55-57); and

a switching structure (figure 1, item 1; column 8, lines 51-63) having a first terminal coupled to an output of a first voltage source (figure 1, item 5; column 8, line 63 to column 9, line 11) and a second terminal coupled to an output of a second voltage source (figure 1, item 6; column 9, lines 12-31), the switching structure containing circuitry to electrically couple the outputs together based on a value on a control signal line (figure 1, item 2; column 9, lines 32-35).

5. Claims 1-5, 7, 9, 11 and 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown (US 5,672,958).

With respect to claim 1, Brown discloses a circuit comprising:

two voltage sources (figure 1, items PS1 and PS2; column 3, lines 49-52); and

a switching structure (figure 1, item 106; column 4, lines 26-34) having a first terminal coupled to an output of a first voltage source (source is coupled to PS1; column 4, lines 50-52) and a second terminal coupled to an output of a second voltage source (drain is coupled to PS2; column 4, lines 52-54), the switching structure containing circuitry to electrically couple the outputs together based on a value on a control signal line (figure 1, item 112; column 4, lines 55-58).

The two switching structures disclosed in Brown are separately controlled. One may be adjusted without influencing the other. Brown discloses that with one switching structure fully on, the control circuit adjusts the second switching structure to produce a voltage level equal to the first (column 5, lines 17-32). The fully on switching structure is analogous to a short circuit or direct conducting power line. The controlled switching structure, therefore, may be controlled to coupled/decoupled the outputs of the two power sources.

With respect to claim 2, Brown discloses the circuit of claim 1, and further discloses when the switching structure is off, then the outputs are decoupled (column 4, lines 62-67). Further, it is inherent, by the definition of a switching structure that the switch operates in an open or a closed position. The Brown control circuit (114) may deactivate the switch (106) to decouple the power sources (PS1 and PS2).

With respect to claim 3, Brown discloses the circuit of claim 1, and further discloses each of the two voltage sources produce an output of equal voltage potential (column 3, lines 63-66; column 5, lines 17-32).

With respect to claim 4, Brown discloses the circuit of claim 1, and further discloses the switching structure is a transistor (column 4, lines 30-34), the first terminal is the transistor's source, and the second terminal is the transistor's drain. Figure 1 in Brown shows the source and drain of transistor (106) as being coupled to the power sources (PS1 and PS2).

With respect to claim 5, Brown discloses the circuit of claim 4, and further discloses the control signal line is coupled to the transistor's gate (figure 1; column 4, lines 62-65).

With respect to claims 7, Brown discloses the circuit of claim 4, and further discloses that the transistor is an N-type MOSFET (figure 1, item 106; column 4, lines 58-62).

With respect to claim 9, Brown discloses the circuit of claim 1, and further discloses the voltage sources are used to power separate power domains (column 3, lines 63-65). The Brown circuit comprises two power supplies that output multiple voltage levels to power separate power domains.

With respect to claim 11, Brown discloses the circuit of claim 1, and further discloses each of the two voltage sources comprises a voltage supply (figure 1, items PS1 and PS2) controlled by a switch (figure 1, items S1 and S2; column 3, line 66 to column 4, line 2; column 6, lines 26-37). Brown discloses that switches (S1, S2) are used to determine the feedback sensing point to control and regulate the power supplies.

With respect to claim 16, Brown discloses the circuit of claim 1, and further discloses each voltage source has an independent voltage supply (figure 1, items PS1 and PS2).

With respect to claim 17, Brown discloses the circuit of claim 1, and further discloses the switching structure reduces turn on current spikes. It is inherent that the

Brown switching structure would reduce turn on current spikes, since the Brown switching structure is identical to applicants'.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6, 8, 10, 12-15 and 18-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown.

With respect to claim 6, Brown discloses the circuit of claim 4, and further, it would have been obvious to one skilled in the art that the Brown N-type MOSFET maybe replaced with a P-type MOSFET. Brown discloses that the feedback switches may be either N or P-type (column 3, lines 11-13). Further, it is known in the art that N-type and P-type MOSFETs are interchangeable as switching structures. The two transistors simply require opposite control inputs at the gate to switch on/off.

With respect to claim 8, Brown discloses the circuit of claim 4, but does not expressly disclose the transistor is made from thick oxide to provide low-leakage characteristics. At the time of the invention by applicants, it would have been obvious to one skilled in the art to utilize a low-leakage transistor. Any transistor with high-leakage characteristics would not function well as a switch since it would not adequately turn fully on or off.

With respect to claim 10, Brown discloses the circuit of claim 1, and further, it would have been obvious to one skilled in the art that Brown discloses the voltage sources are used to power sub-domains within a single power domain. Brown discloses that the load is a computer or other electronic device (column 3, lines 45-52). Computers commonly comprise power domains and sub-domains and it would have been obvious that the Brown circuit supplies power to these sub-domains.

With respect to claim 12, Brown discloses the circuit of claim 11, and further discloses wherein the switch in each voltage source is a transistor (figure 2, item 202, 206, 212, 216; column 7, line 60 to column 8, line 32) and wherein the switching structure is a transistor (column 4, lines 30-34). Brown does not expressly disclose the width of the transistors in each voltage source are approximately equal and the width of the transistor in the switching structure is on the order of 10 to 20 percent the width of the transistors in the voltage sources. At the time of the invention by applicants, it would have been obvious to one skilled in the art to select a switching structure transistor with a 10-20% width of the voltage source transistors, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

With respect to claims 13 and 14, Brown discloses the circuit of claim 12 and further discloses the voltage source transistors and the switching structure transistors are N-type MOSFETs or P-type MOSFETs, as discussed above in the rejections of claims 6 and 7.

With respect to claim 15, Brown discloses the circuit of claim 1, and further it would be obvious to one skilled in the art that the Brown circuit discloses the voltage sources share a common voltage source. Brown discloses that the load may comprise a computer, or other electric device which would require that the user plug the load into an electrical outlet for power. The electrical power supplied by the utility grid would therefor, supply both PS1 and PS2 with power.

With respect to claim 18, Brown discloses M voltage sources (figure 1, items PS1 and PS2; column 3, lines 49-52), and a switching network having M terminals (figure 1, items 104, 124), wherein each terminal is coupled to an output from one of the M voltage sources, the switching network containing circuitry to electrically couple the outputs of the M voltage sources (figure 1, items 106, 126; column 4, lines 26-34), wherein the coupling of the outputs is based on a mapping.

As discussed above, the mapping is interpreted as a simple, predetermined coupling of all of the voltage sources.

Brown does not expressly disclose M is an integer number greater than two. At the time of the invention by applicants, it would have been obvious to one skilled in the art to use more than two voltage sources, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (CCPA 1977).

With respect to claim 19, Brown discloses the circuit of claim 18, and further discloses some of the voltage sources produce outputs with the same voltage potential (column 3, lines 63-65).

With respect to claim 20, Brown discloses the circuit of claim 19, and further discloses the outputs of the voltage sources coupled together all have the same voltage potential (figure 1; column 3, lines 63-66). Brown discloses that the power sources may output multiple voltages, but only the outputs of the same voltage potentials are coupled together.

With respect to claim 21, Brown discloses the circuit of claim 19, and further discloses the switches couple the outputs (figure 1, items 106, 126), and wherein outputs with different voltage potentials are not connected by switches (column 3, lines 63-65). It would be obvious to one skilled in the art that since the common voltage outputs of the Brown power sources are coupled, the different voltage potentials would not be coupled.

With respect to claim 22, Brown discloses the circuit of claim 18, and further discloses the mapping is stored in a memory (figure 1, item 114; column 4, lines 62-67).

With respect to claim 23, Brown discloses the circuit of claim 18, and further discloses the mapping is dynamically computed (column 5, lines 1-16).

With respect to claim 24, Brown discloses the circuit of claim 18, and further discloses switches couple the outputs (figure 1, items 106, 126), and wherein the mapping specifies the state of each switch in the switching network (column 5, lines 1-16).

With respect to claim 25, Brown discloses the circuit of claim 18, and further discloses each output is connected to each other output via a switch (figure 1, items, 106, 126). It would be obvious that with a plurality of redundant power sources, the

Brown circuit would comprise the same number of switches to couple the sources to each other.

With respect to claim 26, Brown discloses the circuit of claim 18, and further, it would have been obvious to one skilled in the art that the Brown discloses each output is connected to two other outputs via a switch. As discussed above, it would be obvious that the Brown circuit may comprise more than 2 power sources. In the embodiment in which the Brown circuit comprises 3 power sources, each source output would be connected to two other outputs via a switch (figure 1, item 106).

With respect to claim 27, Brown discloses the circuit of claim 26, but does not expressly disclose the outputs are connected in a circular fashion. At the time of the invention by applicants, it would have been obvious to one of ordinary skill in the art to connect the outputs in a circular fashion, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA 1950).

With respect to claim 28, Brown discloses the circuit of claim 18, but does not expressly disclose the M voltage sources supply power to M power domains. At the time of the invention by applicants, it would have been obvious to one of ordinary skill in the art to use M voltage sources to supply power to M power domains, since it has been held that rearranging parts of an invention involves only routine skill in the art. *Id.*

With respect to claim 29, Brown discloses the circuit of claim 18, but does not expressly disclose the M voltage sources supply power to M power sub-domains within a single power domain. As discussed above in the rejection of claim 10, it would have

been obvious that the Brown power sources supply power to sub-domains within the load. Further, it would haven been obvious to use M voltage sources to supply power to M sub-domains.

With respect to claim 30, Brown discloses the circuit of claim 18, and further discloses the switching network comprises a plurality of switching structures (figure 1, item 106; column 4, lines 26-34), each switching structure coupling two outputs of equal voltage potential together (column 3, lines 63-65; column 4, lines 16-18), the switching structure comprising:

a first terminal coupled to an output of a first voltage source (source is coupled to PS1; column 4, lines 50-52);

a second terminal coupled to an output of a second voltage source (drain is coupled to PS2; column 4, lines 52-54); and

the switching structure containing circuitry to electrically couple the outputs together based on a value on a control signal line (figure 1, item 112; column 4, lines 55-58).

As discussed above in the rejection of claim 1, Brown discloses that the switch (106) may be controlled to couple the first power source (PS1) to the fully on second power source (PS2). Further, Brown discloses that the embodiment shown in figure 1 is repeated for the multiple voltage outputs of the power sources (column 3, lines 63-65). Each Brown switching structure couples the two outputs of equal voltage together (5v to 5v, 12v to 12v, etc.).

With respect to claim 31, Brown discloses the circuit of claim 30, and further discloses the switching structure is a transistor (column 4, lines 30-34), the first terminal is the transistor's source, and the second terminal is the transistor's drain. Figure 1 in Brown shows the source and drain of transistor (106) as being coupled to the power sources (PS1 and PS2).

With respect to claim 32, Brown discloses an integrated circuit (100) comprising:

a circuitry block (figure 1, RL; column 3, lines 45-52); and

a plurality of power supplies (figure 1, items PS1 and PS2; column 3, lines 49-52 and 63-65), each coupled to the circuitry block, each power supply comprising:

M voltage sources (figure 1, item PS1 and PS2), wherein M in an integer number greater than one; and

a switching network (figure 1, items 104, 124) having M terminals, wherein each terminal is coupled to an output from one of the M voltage sources, the switching network containing circuitry to electrically couple the outputs of the M voltage sources (figure 1, items 106, 126; column 4, lines 26-34), wherein the coupling of the outputs is based on a mapping.

The plurality of power supplies disclosed in Brown is the set of power supplies for each voltage potential (column 3, lines 63-65), and each power supply then comprises two sources (PS1, PS2). The mapping is disclosed by Brown as discussed above in the rejection of claim 18.

With respect to claim 33, Brown discloses the integrated circuit of claim 32, but does not expressly disclose the circuitry block comprises a plurality of circuit blocks, and wherein the there is at least one power supply associated with each circuit block. As discussed above in the rejection of claim 10, it would have been obvious that the at least one Brown power sources supply power to a plurality of circuit blocks (sub-domains) within the load.

With respect to claim 34, Brown discloses the integrated circuit of claim 33, and further discloses all power supplies are identical. Brown discloses that the power supplies (PS1 and PS2) are designed to be redundant sources. It would be obvious to one skilled in the art that sources in a redundant power system would be identical.

With respect to claim 35, Brown discloses the integrated circuit of claim 33, and further discloses each power supply may be designed differently (column 5, lines 17-21). Brown discloses that although the power supplies are meant to be identical, they may be designed differently and produce different outputs.

With respect to claim 36, Brown discloses the integrated circuit of claim 33, but does not expressly disclose each circuit block and its associated power supply are located adjacent to one another on the integrated circuit. It would have been obvious to one of ordinary skill in the art to rearrange the Brown circuit to place each power supply adjacent to its respective circuit block in order to reduce clutter and power loss, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA 1950).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

McDonnal (US 5,428,523) discloses a switching structure to couple/decouple parallel sources (DC/DC converters).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on weekdays, from 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

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PRIMARY EXAMINER